Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus, comprising:

two or more memories, wherein each memory has an intelligence wrapper bounding that memory;

a processor to initiate a Built in Self Test for the memories; and

a serial bus coupled between the processor and each memory; wherein the processor loads a command ~~containing representations of a march element and data~~ via the serial bus, wherein the command comprises representations of a march element and data.

2. (Original) The apparatus of claim 1, wherein a first intelligence wrapper contains control logic to decode the command from the processor and to execute a set of test vectors on a bounded memory.

3. (Original) The apparatus of claim 1, wherein the command containing representations of the march element and data is coded in a compressed format and a control logic is configured to expand the representation of the march element and the data.

4. (Original) The apparatus of claim 3, wherein the control logic comprises a state machine configured to decode the command and to execute a set of test vectors.

5. (Original) The apparatus of claim 2, wherein a state machine expands the representations of march elements and data in the command to their full-uncompressed form.

6. (Currently Amended) The apparatus of claim 5, wherein the representation ~~may be~~ comprises a cipher that can be looked up in a data table to determine the uncompressed bits and operations that correspond to the compressed information.

7. (Original) The apparatus of claim 1, wherein the two or more memories share the processor.

8. (Original) The apparatus of claim 1, wherein logic contained in the intelligence wrapper operates at a clock speed asynchronous to a clock speed of the processor.

9. (Original) The apparatus of claim 1, wherein the command further comprises:

input data, expected output data, and address information on where to apply data to addresses in the memories.

10. (Original) The apparatus of claim 1, wherein a structure of the command comprises various blocks of interrelated information.

11. (Currently Amended) The apparatus of claim 1, wherein a structure of the command comprises a series of bits and a position of a bit within ~~that string of sequential~~ the series of bits associates that bit with a particular section of information.

12. (Currently Amended) An apparatus, comprising:

two or more memories, each memory has an intelligence wrapper bounding that memory; and

a processor to initiate a Built In Self Test for the memories, wherein a first intelligence wrapper contains control logic to decode a compressed command from the processor and to execute a set of test vectors on a bounded memory, wherein the processor sends a command based self test to the first intelligence wrapper at a first speed and the control logic executes the operations associated with that command at a second speed asynchronous with the first speed.

13. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper operates at a clock speed greater than the clock speed of the processor.

14. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper further comprises data comparison logic configured to compare actual vectors at an output of a first bounded memory.

15. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper further comprises address generation logic to generate coordinates of a memory word line to be tested.

16. (Original) The apparatus of claim 12, wherein the logic in the intelligence wrapper further comprises data generation logic to expand a representation of data input from the processor to generate a sequence of data to be tested for that particular memory.

17. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper further comprises a state machine configured to decompress the command sent from the processor.

18. (Original) The apparatus of claim 12, wherein a march element in the command may instruct logic in the intelligence wrapper to conduct two or more operations back to back.

19. (Original) The apparatus of claim 1, wherein less than seven routing paths for self test purposes exist between the processor and the bounded memory to be tested.

20. (Original) The apparatus of claim 12, wherein the processor loads the command containing representations of a march element and data to the first intelligence wrapper via a serial bus.

21 (Currently Amended) A machine readable medium that stores data representing an integrated circuit, comprising:

two or more memories, each memory has an intelligence wrapper bounding that memory;

a processor to initiate a Built In Self Test for the memories, wherein a first intelligence wrapper contains control logic to decode a compressed command from the processor and to execute a set of test vectors on a bounded memory, wherein the processor sends a command based self test to the first intelligence wrapper at a first speed and the control logic executes the operations associated with that command at a second speed asynchronous with the first speed.

22. (Original) The machine-readable medium of claim 21, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the memories and the processor.

23. (Original) The machine readable medium of claim 22, wherein the processor loads the command containing representations of a march element and data to the first intelligence wrapper via a serial bus.

24. (Original) The machine readable medium of claim 22, wherein less than seven routing paths for self test purposes exist between the processor and the bounded memory to be tested.

25. (Currently Amended) A method, comprising:

compressing information used in a self test of a memory embedded on a chip; and

communicating the compressed information ~~in a serial manner~~ via a serial bus to logic bounding the ~~memory;~~ memory.

26. (Original) The method of claim *25,* further comprising:

expanding the compressed information to perform the self-test on one or more addresses in the memory.

27. (Original) The method of claim 25, further comprising:

performing operations of the self-test asynchronously with the communication of the compressed information.

28. (Currently Amended) An apparatus, comprising:

means for compressing information used in a self test of a memory embedded on a chip; and

means for communicating the compressed information ~~in a serial manner~~ via a serial bus to logic bounding the ~~memory;~~ memory.

29. (Original) The apparatus of claim 28, further comprising:

means for expanding the compressed information to perform the self-test on one or more addresses in the memory.

30. (Original) The apparatus of claim 28, further comprising:

means for performing operations of the self-test asynchronously with the communication of the compressed information.